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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,167	08/30/2004	Mahmoud A. Mousa	BUR920040020US1	5166

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EXAMINER	
CHIU, TSZ K	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,167	MOUSA ET AL.	
	Examiner	Art Unit	
	Tsz K. Chiu	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see page 5-9, filed May 16, 2006, with respect to the rejection(s) of claim(s) 14-24 under 35 USC 102 and 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bhattacharyya (2004/0144979) in view of Yoshikawa et al. (5,384,473).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya in view of Yoshikawa et al. (5,384,473).

With respect to claim 14, Bhattacharyya discloses a lower semiconductor device (Fig. 10) having an active region (26, For example Fig. 10) comprising a semiconductor with a first crystal orientation, and an upper semiconductor device (Fig. 9) having an active region (26, For example Fig. 9) comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor (Fig. 10) a is formed separately from the lower semiconductor device (Fig. 9) and connected device thereto by an interconnect structure (120, For example Fig. 11).

However, Bhattacharyya did not discloses the first and second orientation.

Yoshikawa discloses the first and second orientation (column 3, lines 57-64).

Since Bhattacharyya and Yoshikawa are both from the same field of endeavor improve CMOS technology, the purpose disclosed by Yoshikawa would have been recognized in the pertinent art of Bhattacharyya.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have use Yoshikawa's crystal orientation for the purpose of first and second surface orientation portions, respectively, makes it possible to maximize the performance of those semiconductor elements of different conductivity types at the same time.

With respect to claim 15, Bhattacharyya discloses invention set forth to claim 1, but did not disclose the first crystal orientation is different from the second crystal orientation.

Yoshikawa discloses the first crystal orientation is different from the second crystal orientation (column 1, liens 46-53).

Since Bhattacharyya and Yoshikawa are both from the same field of endeavor improve CMOS technology, the purpose disclosed by Yoshikawa would have been recognized in the pertinent art of Bhattacharyya.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have use Yoshikawa's different orientation in the active region in Bhattacharyya's invention for the purpose of different conductivity types in the first and second surface orientation portions, respectively, makes it possible

to maximize the performance of those semiconductor elements of different conductivity types at the same time.

With respect to claim 16, Bhattacharyya discloses at least one layer of a semiconductor device (120, For example Fig. 11) between the lower and upper semiconductor devices (Fig. 11).

With respect to claim 17, Bhattacharyya discloses at least one semiconductor device of the at least one layer of semiconductor device (120, For example Fig. 11) comprises an active region (144,142, For example Fig. 11) having a crystal orientation different from the crystal orientation (110, For example Fig. 11) of at least any one of the lower semiconductor device (bottom half of the device in Fig. 11) and the upper semiconductor device (top half of the device in Fig. 11).

With respect to claim 18, Bhattacharyya discloses the upper semiconductor device (top half of the device in Fig. 11) is bonded to the top of the lower semiconductor device (bottom half of the device in Fig. 11) with an insulating layer (120, For example Fig. 11), and wherein at least a portion of the upper semiconductor device (top half of the device in Fig. 11) is electrically connected to at least a portion of the lower semiconductor device (bottom half of the device in Fig. 11).

With respect to claim 19, Bhattacharyya discloses the lower semiconductor device (bottom half of the device in Fig. 11) include either a pFET device or an nFET device, and the upper semiconductor device (top half of the device in Fig. 11) includes either a PFET device or an nFET device,

Yoshikawa discloses the crystal orientation of the-active region of the respective lower semiconductor device is different from the crystal orientation of the active region of the respective upper semiconductor device (column 1, liens 46-53).

With respect to claim 20, Bhattacharyya discloses the lower and upper semiconductor devices comprise an inverter (fig. 11)

Yoshikawa discloses the PFET device has a crystal orientation of (100) in an active region and the n/ET device has a crystal orientation of (110) in an active region (column4, lines 6-9).Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 517-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TKC

Zandra V. Smith
Supervisory Patent Examiner
24 July 2007

July 23, 2006